ACKNOWLEDGMENT

The authors wish to thank C. B. Winn who helped with the measurements.

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Design of GaAs MESFET Oscillator Using Large-Signal *S*-Parameters

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***Abstract*—A design method of GaAs MESFET oscillator using large-signal *S*-parameters has been discussed. Together with the measurement results of the dependence of large-signal *S*-parameters on power levels and bias conditions, computer analysis of the equivalent circuit for MESFET's has qualitatively clarified the large signal properties of MESFET's. On the basis of these findings, *S*-parameters have been designed for the MESFET oscillator over the frequency range of 6–10 GHz, which has resulted in power output of 45 mW at 10 GHz with 19-percent efficiency, and 350 mW at 6.5 GHz with 26-percent efficiency, respectively.**

Good agreements between predicted and obtained performances of MIC positive feedback oscillator have been ascertained, verifying the validity of the design method using large-signal *S*-parameters.

I. INTRODUCTION

EXCELLENT performances of GaAs Schottky gate-field effect transistors (GaAs MESFET's) in frequency [1], [2] and power [3]–[5] have provoked microwave systems engineers to design GaAs MESFET oscillators [6]–[8] as a local oscillator or a microwave power source. Since microwave oscillators using GaAs MESFET's operate under a large-signal condition, circuit designers have been forced to utilize cut and try methods to achieve the optimum design, modifying the design with small-signal *S*-parameters.

This paper describes a successful design method of low-noise GaAs MESFET oscillators using measured large-signal *S*-parameters [9]. In Section II, the measurement and applicability of large-signal *S*-parameters of *X*-band GaAs MESFET are represented, and, together with the equivalent circuit analysis, large-signal properties of FET's are discussed qualitatively. Then some of the limitations of large-signal *S*-parameters on the design of the oscillator are deduced. The detailed design considerations of oscillators are presented in Section III. In Section IV, some experimental results of designed oscillators are shown, and good agreements between predicted and obtained performances are ascertained, verifying the validity of the design method using large-signal *S*-parameters.

Manuscript received May 16, 1977; revised July 3, 1977.
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II. LARGE-SIGNAL *S*-PARAMETERS

Each transistor used in this experiment has a 1-μm long and 300-μm wide gate, a channel doping of 7–9 $\times 10^{16}$ cm^{-3} and pinch-off voltage of 4.0 V nominally, which is mounted in a microdisk package.

Large-signal *S*-parameters, if measured, could be used to calculate gate and drain RF current amplitudes $|\tilde{i}_{gs}|$ and $|\tilde{i}_{ds}|$ as a function of the available power of signal generator P_I:

$$P_I = |a_i|^2, \qquad i = 1, 2 \tag{1}$$

$$S_{11} = \left(\frac{b_1}{a_1}\right)_{a_2=0} = \frac{Z_{L1} - Z_0}{Z_{L1} + Z_0} \tag{2}$$

$$P_I(1 - |S_{11}|^2) = \tfrac{1}{2}\,\mathrm{Re}\,(Z_{L1})|\tilde{i}_{gs}|^2 \tag{3}$$

$$S_{22} = \left(\frac{b_2}{a_2}\right)_{a_1=0} = \frac{Z_{L2} - Z_0}{Z_{L2} + Z_0} \tag{4}$$

$$P_I(1 - |S_{22}|^2) = \tfrac{1}{2}\,\mathrm{Re}\,(Z_{L2})\,|\tilde{i}_{ds}|^2 \tag{5}$$

where Z_{L1}, Z_{L2} are the input and the output impedances of FET and $Z_0 = 50\ \Omega$.

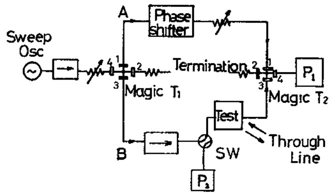

Fig. 1. Block-diagram of the measurement system for $\angle S_{12}, \angle S_{21}$.

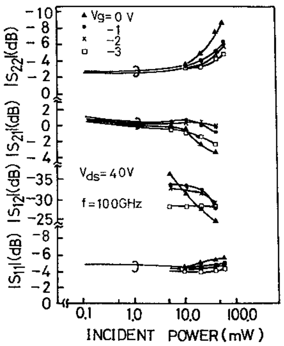

Fig. 2. Dependence of the amplitude of the S-parameters on the incident power level.

Large signal S-parameters of this device have been measured under class A or AB operation by a standing-wave method for S_{11}, S_{22}, by a direct observation of transmission power for $|S_{12}|, |S_{21}|$, and by a magic T method for $\angle S_{12}, \angle S_{21}$, the block diagram of which is shown in Fig. 1. The power levels have been from -10 dBm to 20 dBm over the frequency range of 6.0–10.0 GHz. In these ranges, harmonic components were scarcely observed at both input and output terminals.

Fig. 2 shows the typical results of measured amplitudes $|S_{ij}|$'s plotted versus incident power levels at 10 GHz. As for the phase angles, no significant variations were detected. The amplitude changes versus signal levels are relatively small for the input parameters $|S_{11}|, |S_{21}|$ compared to those for output ones $|S_{22}|, |S_{12}|$, when gate is biased in the range of $V_p/2 \pm 1.0$ V.

Computer analysis [10] of the well-known lumped-element equivalent circuit for MESFET's has clarified that the remarkable changes of $|S_{22}|$ and $|S_{12}|$ with the increase of power level, as indicated in Fig. 2, are mainly due to the increase of drain conductance r_d, and feedback capacitance C_{gd}. The calculated dependence of these components on the S-parameters are shown in Fig. 3.

On the basis of these results, we approximated that the input parameters S_{11}, S_{21} and the output parameters S_{22}, S_{12} measured under equal power levels could be treated as a set of S-parameters. In this case, S_{ij} can be expressed as a function of the drain current amplitude $|\tilde{i}_{ds}|$, i.e.,

$$S_{ij} = S_{ij}(V_{ds}, V_{gs}(V_p \pm 1.0 \text{ V}), f_1, |\tilde{i}_{ds}|). \quad (6)$$

III. Oscillator Design

Using these large signal S-parameters, the parallel feedback FET oscillator with common source has been designed over the frequency range of 6.0–10.0 GHz, which is, as

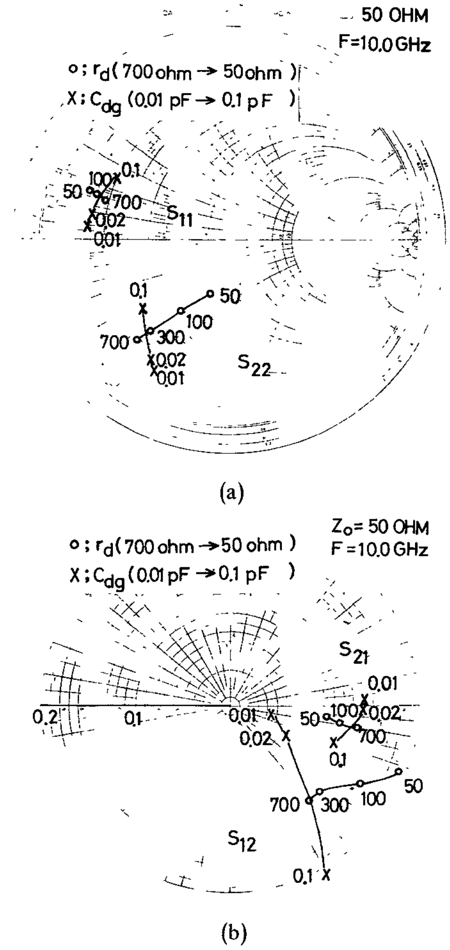

Fig. 3. Calculated dependences of the drain conductance and the feedback capacitance on the S-parameters.

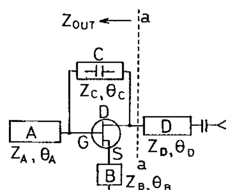

Fig. 4. FET feedback oscillator configuration.

indicated in Fig. 4, composed of an input matching circuit (characteristic impedance Z_A, electric length θ_A), a short transmission line between source and earth (Z_B, θ_B), a feedback network from drain to gate (Z_C, θ_C), and an output matching circuit (Z_D, θ_D). This oscillator contains a series feedback element, corresponding to Fig. 4(b).

Design procedure is as follows. Output impedance at drain terminal ($Z_{\text{out}} = -R_0 + jX_0$) is calculated as the function of Z_A, Z_B, Z_C, θ_A, θ_B, θ_C and the large signal S-parameters. Fig. 5 illustrates the contour lines of zero negative resistance at each power level calculated as a function of θ_A, θ_C, in the case of $f = 10.0$ GHz, $Z_A, Z_C = 50\ \Omega$, $Z_B = 30\ \Omega$, $\theta_B = \pi/12$. The shaded area in the figure represents the negative resistance region. As the power level in the

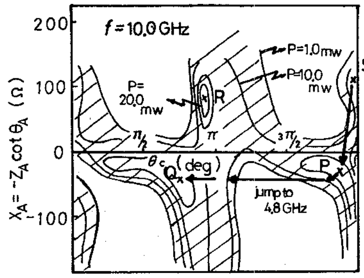

Fig. 5. Calculated negative resistance area as a function of θ_A,θ_C and the large signal S-parameters.

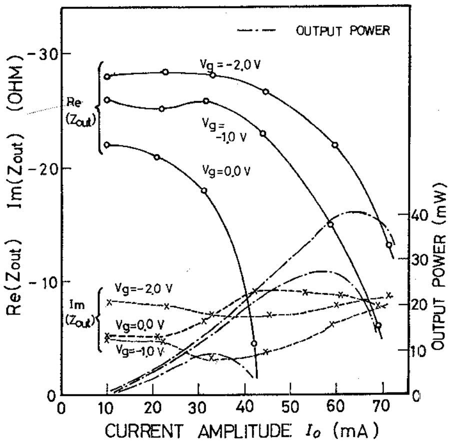

Fig. 6. Dependence of Z_{out} on the RF current amplitude and the calculated power.

S-parameters measurement increases, the negative resistance region shrinks toward points P, Q, and R. In this circuit configuration, an area where the maximum negative resistance is obtained at the small-signal level, does not necessarily mean a condition of stable oscillation. We have adopted the circuit condition of either P, Q, or R as the optimum design point of the FET oscillator.

Fig. 6 shows the dependence of Re (Z_{out}) $(= -R_0)$ and Im (Z_{out}) $(= X_0)$ on the RF output current amplitude $|\tilde{i}_0|$ calculated at the point Q in Fig. 5. $|\tilde{i}_0|$ is the difference of $|\tilde{i}_{ds}|$ and $|\tilde{i}_{gs}|$, i.e.,

$$|\tilde{i}_0| = |\tilde{i}_{ds}| - |\tilde{i}_{gs}| \tag{7}$$

and the maximum available gain $G_0(|\tilde{i}_{ds}|)$ is written as

$$G_0(|\tilde{i}_{ds}|) = \frac{\text{Re }(Z_{L2})|\tilde{i}_{ds}|^2/2}{\text{Re }(Z_{L1})|\tilde{i}_{gs}|^2/2} \tag{8}$$

then

$$|\tilde{i}_{gs}| = \sqrt{\frac{1}{G_0}\frac{\text{Re }(Z_{L2})}{\text{Re }(Z_{L1})}}\,|\tilde{i}_{ds}|. \tag{9}$$

Since the feedback term S_{12} is sufficiently small as shown in Fig. 2, we have set it equal to zero. In the unilateral case [11], (8) is expressed as

$$G_0 = \frac{|S_{21}|^2}{|1 - |S_{11}|^2|\,|1 - |S_{22}|^2|} \tag{10}$$

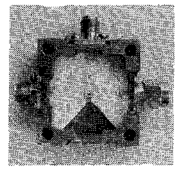

Fig. 7. Photograph of an integrated X-band FET oscillator.

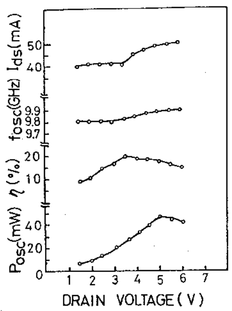

Fig. 8. Microwave performance of X-band GaAs MESFET.

and the current amplitude $|i_0|$ can be written from (7), (9), and (10)

$$|\tilde{i}_0| = \left(1 - \sqrt{\frac{|1 - |S_{11}|^2|\,|1 - |S_{22}|^2|}{|S_{21}|^2}\frac{\text{Re }(Z_{L2})}{\text{Re }(Z_{L1})}}\right)|\tilde{i}_{ds}| \tag{11}$$

$|\tilde{i}_0|$ is calculated with large signal S-parameters and specified $|\tilde{i}_{ds}|$.

From Fig. 6, it is found that $-R_0$ does not decrease linearly with the increase of $|\tilde{i}_0|$ and the change of X_0 is relatively small, because of the slight variation of $\angle S_{ij}$. From Fig. 6, the optimum load condition (Z_D,θ_D) are determined and the oscillation power and efficiency are estimated.

IV. Experimental Results

On the basis of the above mentioned procedure, oscillator circuits have been fabricated on alumina ceramic substrates. A photograph of one of the fabricated oscillators is shown in Fig. 7.

When the circuit elements have been adjusted to points S,P,Q in turn in Fig. 5, maximum oscillation powers have been obtained near the point P ($f = 9.95$ GHz, $P_{out} = 45$ mW, $\eta = 19.1$ percent) and the point Q ($f = 10.05$ GHz, $P_{out} = 38$ mW, $\eta = 16.2$ percent). These results almost agree with the predicted powers and frequencies from Fig. 5. Fig. 8 shows the output power, efficiency, oscillation frequency, and drain current as the function of drain voltage for the oscillator corresponding to the point Q.

As for the frequency sensitivity of the oscillator-to-drain and gate bias, $\Delta f/\Delta V_{ds} \simeq 10$–$30$ MHz/V and $\Delta f/\Delta V_{gs} \simeq 70$ MHz are obtained, respectively.

Noise performances of these oscillators have also been measured. The FM and AM noise were -74 dB/Hz ($Q_{ex} \simeq 40$) and -156 dB/Hz, respectively, for the offcarrier frequency of 10 kHz at the point Q, which are comparable to those of a Gunn oscillator.

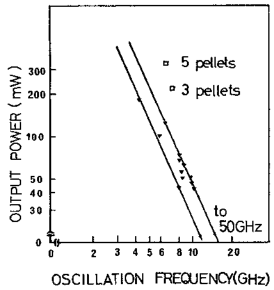

Fig. 9. Frequency dependence of maximum oscillation powers obtained with several kinds of FET samples.

Several oscillators with center frequencies from 6 to 10 GHz have also been designed, and an output power of 350 mW with 26-percent efficiency at 6.5 GHz have been obtained using five chips in parallel combination, in this case, the effective gate width is 1500 μm.

Frequency dependence of maximum-oscillation powers obtained with several kinds of FET samples indicates that the extrapolation leads to about 50 GHz, which is the maximum oscillation frequency of the device, as shown in Fig. 9.

V. Conclusion

FET for an oscillator design should be characterized by large-signal S-parameters, which are to be expressed as a function of drain current amplitude $|\tilde{i}_{ds}|$ and gate current amplitude $|\tilde{i}_{gs}|$.

A design method for MESFET oscillators has been developed by taking these current amplitudes into consideration.

Predicted powers and frequencies have been obtained from fabricated MIC oscillators over the frequency range of 6 to 10 GHz, verifying the validity of the design method using large-signal S-parameters.

Acknowledgment

The authors wish to thank T. Ishii, T. Oda, and H. Kumabe for the fabrication of FET's. They also thank Dr. H. Miki, Dr. T. Yahara, Dr. M. Otsubo, and Dr. M. Kotani for their useful assistances and suggestions.

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